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⑤4 Integrator circuit.

57) The integrator circuit uses switched current techniques and comprises a first current memory cell (T31,T32,S31,C31) a second current memory cell (T33,T34,C32,S32,T35) and a third (correcting) current memory cell (T36,S33,C33). An input current signal is fed to input (30) and switch (S30) is closed during the $\bar{\phi}$ portion of each sampling period as is the switch (S31) in the first current memory cell. The other switches (S32,S33) are closed during the ϕ portion of each sampling period. During the ϕ portion transistor (T31) acts as a current source producing the current applied to it in the preceding $\bar{\phi}$ portion. This is subtracted from the current produced by the output of the second current memory cell (T34) and the difference stored in the third current memory cell (T36,S33,C33). During the next $\bar{\phi}$ portion transistor T36 acts as a current source correcting the feedback current fed to the input (T31) of the first current memory cell. This reduces the sensitivity of the integrator to device matching.

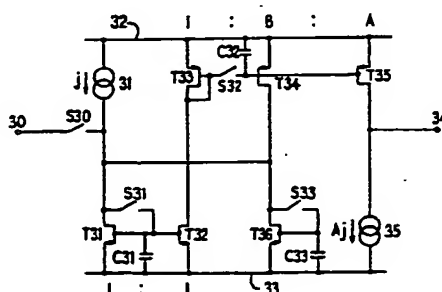


FIG. 3

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INTEGRATOR CIRCUIT

The invention relates to an integrator circuit for integrating an input signal in the form of a sampled analogue current, the integrator comprising input means for receiving the input signal, output means for producing as an output signal the integrated input signal, a current memory cell for producing at its output during a first portion of each sampling period a current related to that applied to its input during a second portion of that or a preceding sampling period, means for coupling the output of the current memory cell to the integrator output means, and feedback means for applying a feedback signal to the input of the current memory cell during the second portion of each sampling period.

An integrator circuit as set forth in the preceding paragraph has been disclosed in a paper by J. B. Hughes, N. C. Bird, and I. C. Macbeth entitled "Switched Currents - A New Technique for Analogue Sampled-Data Signal Processing" which was presented to The Institution of Electrical Engineers on 17th February 1989.

Figure 1 illustrates an integrator circuit as set forth in the opening paragraph while Figure 2 shows the clock waveforms used to operate the switches in the circuit of Figure 1.

The integrator circuit shown in Figure 1 has an input 1 which is connected to the junction of a current source 2 and the drain electrode of an n-channel field effect transistor T1. The other end of the current source 2 is connected to a positive supply rail 3 while the source electrode of transistor T1 is connected to a negative supply rail 4. The drain electrode of transistor T1 is connected to its gate electrode and to one end of a switch S1. The other end of the switch S1 is connected to the junction of a capacitor C1 and the gate electrode of an n-channel field effect transistor T2. The source electrode of transistor T2 and the other end of the capacitor C1 are connected to the negative supply rail 4. The drain electrode of transistor T2 is connected to the drain electrode of a p-channel field effect transistor T3 whose source electrode is connected to the positive supply rail 3. The drain electrode of transistor T3 is connected to its gate electrode and to one end of a switch S2. The other end of the switch S2 is connected to the junction of the gate electrode of a p-channel field effect transistor T4 and a capacitor C2. The source electrode of transistor T4 and the other end of capacitor C2 are connected to the positive supply rail 3. The gate electrode of transistor T4 is further connected to the gate electrode of a p-channel field effect transistor T6 whose source electrode is connected to the positive supply rail 3. The drain electrode of transistor T4 is connected to the drain electrode of an n-channel field effect transistor T7 whose source electrode is connected to the negative supply rail 4 and via a feedback connection 10 to the drain electrode of transistor T1. A current source 9 is connected between the positive supply rail 3 and the drain electrode of an n-channel field effect transistor T10 whose source electrode is connected to the negative supply rail 4. The drain electrode of transistor T10 is connected to its gate electrode, to the gate electrode of transistor T7, and to the gate electrode of an n-channel field effect transistor T9. The source electrode of transistor T9 is connected to the negative supply rail 4 while its drain electrode is connected to the drain electrode of transistor T6 and to an output terminal 7.

The operation of the circuit shown in Figure 1 is as follows. Input 1 is fed by a current i which is a sampled current and remains substantially constant during each sampling period and changes in successive sampling periods to follow the continuous analogue signal from which it is derived. A feedback current i_f , which is the difference between the currents produced by transistors T4 and T7, is produced in the feedback path 10 while an output current i_o , which is the difference between the currents produced by transistors T6 and T9, is produced at the output 7. The current sources 2 and 9 both produce a bias current j . The ratios of the currents conducted by transistors T3, T4 and T6 are arranged to be 1:B:A, while the ratios of the currents conducted by transistors T10, T9 and T7 are arranged to be 1:A:B. Switch S1 is arranged to be closed during a portion ϕ of each sampling period while switch S2 is arranged to be closed during a non-overlapping portion ϕ of each sampling period.

During the ϕ of sampling period (n-1), see Figure 2, the current $i(n-1)$ is applied to input 1 and this current together with the bias current j produced by current source 2 and a feedback current i_f on line 10 is applied to the input of the first memory cell. As a result a current i_2 is produced by transistor T2 which can be derived from the equation

$$i_2 = i(n-1) + j + i_f$$

where $i_f = i_o(n-1) B/A$
 i.e., $i_2 = i(n-1) + j + i_o(n-1) B/A$.

During the ϕ portion of sampling period n the switch S1 is open but the current i_2 is maintained at its previous value by the charge on capacitor C1. Consequently the current $i_2 = i(n-1) + j + i_o(n-1) B/A$ is fed to the input of the second memory cell and as switch S2 is closed a current i_4 is produced by transistor T4

and a current I_6 is produced by transistor T6. The current I_4 is equal to $B I_2$ while the current I_5 is equal to $A I_2$.

Consequently the current I_5 during the sampling period n is given by the expression

$$I_5(n) = A[i(n-1) + j + i_o(n-1) B/A].$$

5 The current $i_o(n)$ is given by $I_5(n) - A j$.

$$\begin{aligned} \text{Consequently } i_o(n) &= A i(n-1) + A j + A i_o(n-1) B/A - A j \\ &= A i(n-1) + B i_o(n-1). \end{aligned}$$

Converting to the z-domain:

$$i_o(z) = A i(z)z^{-1} + B i_o(z)z^{-1}$$

10 therefore

$$H(z) = \frac{i_o(z)}{i(z)} = \frac{A z^{-1}}{1 - B z^{-1}}$$

15

The continuous time lossy integrator is described by

$$H(s) = \pm \frac{1}{a + s\tau}$$

20

$$\text{Using the forward Euler transform } s \rightarrow \frac{1}{T} \cdot \frac{1 - z^{-1}}{z^{-1}}$$

25

$$H(z) = \pm \frac{T}{\tau} \frac{z^{-1}}{1 - \frac{\tau - aT}{\tau} z^{-1}}$$

30

$$\text{i.e. } A = T/\tau \text{ and } B = \frac{\tau - aT}{\tau}.$$

35 Thus $B = 1$ corresponds to $a = 0$ and gives lossless integration. The integrator shown in Figure 1 can be modified to perform according to the backward Euler transform by connecting the input 1 to the drain electrode of transistor T2 instead of to the drain electrode of transistor T1.

This integrator circuit which is as disclosed in Figure 20 of our co-pending UK patent application no. 8816072.6 (PHB33477) has certain disadvantages. For proper operation it relies on the feedback current i_f being an exact replica of the current applied to the drain electrode of transistor T1 in the preceding sample period (minus the bias current j). However the accuracy of this feedback current can be impaired by a number of factors. First if the gain of the feedback loop becomes greater than unity the system becomes unstable. Conversely if the gain is less than unity the integrator becomes lossy, that is the inverter becomes a first order low pass filter whose cut off frequency becomes highly sensitive to small changes in the gain if the cut off frequency is much less than the clock frequency. The gain of the feedback loop is in turn directly determined by the matching between transistors T1 and T2 and between transistors T3 and T4. Secondly the switches S1 and S2 introduce clock feedthrough which distorts the signal and accumulates in the integrator causing d.c. offsets at the output of the integrator. Thirdly for each of the current memory cells there is a time constant set up due to the $1/g_m$ of the diode connected transistor, the 'on-resistance' of the switch, and the gate capacitance (and additional capacitance if provided) of the output transistor. This filters the signal in the non-linear voltage domain and causes signal distortion. Further a delay determined by this time constant and the frequency of the sampled signal changes the effective value of the unit delay z^{-1} which corrupts the filter characteristics.

45 It is an object of the invention to enable the provision of an integrator circuit in which the effects of one or more of these disadvantages is/are mitigated.

55 The invention provides an integrator circuit as set forth in the opening paragraph characterised in that the feedback means comprises determining means for determining during the first portion of each sampling period the signal current applied to the current memory cell and means for applying a feedback current dependent on the determined current to the input of the current memory cell during the second portion of

each sampling period.

The invention is based on forcing a delayed feedback signal current to assume a known value rather than relying on device matching in current mirror or current memory circuits to produce a correct value of feedback current. Thus the magnitude of the feedback signal can be made insensitive to device matching
 5 reducing the sensitivity of high Q integrators fabricated using switched current techniques to device mismatches.

The current memory cell may comprises a field effect transistor having a switch connected between its drain and gate electrodes, the switch being closed only during the second portion of each sampling period. An additional capacitor may be connected between gate and source electrodes of the transistor.

10 By constructing the current memory cell in this way when the switch is opened the transistor acts as a current source producing the same current as was fed to it when the switch was closed. Since the same transistor is used there will be no device mismatch and hence the current produced during the first portion of a sampling period will be equal to the current applied during the previous second portion of a sampling period (neglecting any clock feedthrough from the switch or charge leakage from the capacitor or
 15 gate/source capacitance).

The means for coupling the output of the current memory cell to the output means of the integrator circuit may comprises a further current memory cell.

This provides a convenient arrangement which enables the time when the output is valid within each sampling period to be determined.

20 The means for applying the feedback current may comprise means for coupling an output of the second current memory cell to the input of the first current memory cell during the second portion of each sampling period.

The output of the second current memory cell will, provided that the correct current ratios are chosen, be of approximately the correct value for the feedback signal and can provide the bulk of the feedback
 25 signal.

The input of a third current memory cell may be coupled to the input of the first current memory cell, the third current memory cell receiving during the first portion of each sampling period the difference between the current produced at the input of the first current memory cell and that produced at the output of the second current memory cell, and supplying that current to the input of the first current memory cell
 30 during the second period of each sampling period.

The third current memory cell corrects the output of the second current memory cell in the feedback path so that the correct feedback signal is applied even when device mismatch is present.

The second current memory cell may have a further output which supplies a scaled version of the current at the first output during the first portion of each sampling period and applies it to the input of the
 35 third current memory cell.

This enables a lossy integrator to be formed since the third current memory cell will now overcorrect the feedback signal causing only a proportion (dependent on the scaling factor of the further output) of the output current to be fed back to the input.

The integrator may further comprise means for adding a bias current to the input signal and means for
 40 subtracting a suitably scaled bias current from the feedback and output signals so that bi-directional input currents can be integrated and bi-directional output currents produced.

This enables the integrator to be formed as a self contained module within a switched current system and to receive and produce bi-directional input and output currents while processing within the module only unidirectional currents so that the input diodes of the current memory and current mirror circuits are
 45 not reverse biased.

The integrator circuit may be arranged such that signal currents are conducted only by field effect transistors having one polarity and may be arranged so that only n-channel field effect transistors conduct signal currents.

As disclosed in our co-pending application No. 8828667.9 (PHB33514), the contents of which are
 50 hereby incorporated by reference, this allows lower supply rail voltages to be used for a given circuit performance.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a circuit diagram of an integrator circuit as disclosed in UK Patent application no.
 55 8816072.6 (PHB33477).

Figure 2 is a timing diagram showing clock waveforms used for operating switches in the integrator circuits described herein.

Figure 3 is a circuit diagram of a first embodiment of an integrator circuit according to the invention,

Figure 4 is a circuit diagram of a second embodiment of an integrator circuit according to the invention,

Figure 5 is a circuit diagram of a third embodiment of an integrator circuit according to the invention,

Figure 6 is a circuit diagram of a fourth embodiment of an integrator circuit according to the invention,

Figure 7 is a circuit diagram of a fifth embodiment of an integrator circuit according to the invention, and

Figure 8 is a circuit diagram of a sixth embodiment of an integrator circuit according to the invention.

Figure 3 shows a first embodiment of an integrator circuit according to the invention which comprises an input 30 which is connected via a switch S30 to the junction of a current source 31 and the drain electrode of an n-channel field effect transistor T31. The other end of the current source 31 is connected to a positive supply rail 32 while the source electrode of transistor T31 is connected to a negative supply rail 33. The drain electrode of transistor T31 is connected via a switch S31 to its gate electrode, to one end of a capacitor C31 whose other end is connected to the negative supply rail 33, and to the gate electrode of an n-channel field effect transistor T32. The drain electrode of transistor T32 is connected to the drain electrode of a p-channel field effect transistor T33 whose source electrode is connected to the positive supply rail 32. The drain electrode of transistor T33 is connected to its gate electrode and to one side of a switch S32 whose other side is connected to the junction of a capacitor C32 and the gate electrodes of two further p-channel field effect transistors T34 and T35. The source electrodes of transistors T34 and T35 and the other end of the capacitor C32 are all connected to the positive supply rail 32. The drain electrode of transistor T34 is connected to the drain electrode of transistor T31 and to the drain electrode of an n-channel field effect transistor T36. The drain electrode of transistor T36 is connected via a switch S33 to its gate electrode and to one end of a capacitor C33. The source electrodes of transistors T32 and T36 and the other end of the capacitor C33 are connected to the negative supply rail 33. The drain electrode of transistor T35 is connected to an output terminal 34 and via a current source 35 to the negative supply rail 33. The capacitors C31, C32, and C33 may be formed by the gate/source capacitance of transistors T32, T34, and T36 respectively or may be additional capacitors. The current source 31 is arranged to provide a current j while the current source 35 is arranged to provide a current $A.j$. Switches S30 and S31 are closed during the portion $\bar{\phi}$ of each sampling period which the switches S32 and S33 are closed during the portion ϕ of each sampling period (see Figure 2).

The operation of the integrator circuit is as follows. During the $\bar{\phi}$ period of sampling period $(n-1)$ a current $i(n-1)$ is applied to input 30 and consequently a current $I_a(n-1)$ equal to $j + i(n-1) + i_f(n-1)$ is applied to the input of the first current memory cell formed by transistors T31 and T32, capacitor C31 and switch S31. At the end of the portion $\bar{\phi}$ switches S30 and S31 open and transistor T31 becomes a current source passing the current $I_a(n-1)$ and transistor T32 also passes a current nominally equal to $I_a(n-1)$. During the portion ϕ of sampling period n switches S32 and S33 are closed and transistor T34, which together with transistor T33, switch S32 and capacitor C32 forms a second current memory cell, conducts a current $I_b(n)$ which is nominally equal to $j + i(n-1) + i_f(n-1)$. However, in practice, the current I_b is unlikely to be precisely equal to the current I_a due to mismatches between transistors T31 and T32 and between transistors T33 and T34, and clock feedthrough effects of switches S31 and S32. Since both transistors T31 and T32 are acting as current sources the difference between the currents $I_a(n-1)$ and $I_b(n)$ plus the current j flows through transistor T36 as a current $I_c(n) = I_a(n-1) - I_b(n) + j$. Transistor T36 together with switch S33 and capacitor C33 acts as a third current memory cell which stores the error current $I_c(n)$. During portion $\bar{\phi}$ of sampling period n the current $i(n)$ is applied to input 30 and the feedback current $i_f(n)$ will be equal to $I_a(n-1) - I_b(n) - I_c(n)$. Thus the feedback current i_f is very close to the required value and is not dependent on the matching between transistors T31 and T32 and between transistors T33 and T34. Also the clock feedthrough effects due to switches S31 and S32 tend to cancel while those due to switches S1 and S2 in Figure 1 accumulate. The accuracy of the feedback signal i_f depends principally on the accuracy with which the current I_c can be retained by transistor T36 and it should be noted that mismatches between the current sources S31 and S35 are not integrated since the bias current present in the output of the second current memory cell due to the effect of current source 31 is cancelled by the bias current component of the output of the third current memory cell which was derived from the current source 31. Thus while mismatches between current sources 31 and 35 will cause an offset error this error is not integrated as would be the case with the circuit of Figure 1.

Figure 4 is a circuit diagram of a lossy integrator according to the invention. The integrator has an input 41 which is connected via a switch S41 to the junction of a current source 42 and the drain electrode of an n-channel field effect transistor T41. The other end of the current source 42 is connected to a positive supply rail 43 while the source electrode of transistor T41 is connected to a negative supply rail 44. The

drain electrode of transistor T41 is connected via a switch S42 to its gate electrode and to the gate electrode of an n-channel field effect transistor T42. A capacitor C42 is connected between the gate electrode of transistor T42 and the negative supply rail 44. The drain electrode of transistor T42 is connected to the drain electrode of a p-channel field effect transistor T43 whose source electrode is connected to the positive supply rail 43. The drain electrode of transistor T43 is connected to its gate electrode and to one side of a switch S43 whose other side is connected to the gate electrodes of three further p-channel field effect transistors T44, T45, and T47. A capacitor C43 is connected between the gate electrode of transistor T41 and the positive supply rail 43. The drain electrode of transistor T44 is connected to the drain electrode of transistor T41 and to the drain electrode of an n-channel field effect transistor T46. The drain electrode of transistor T46 is connected to its gate electrode via a switch S44 while a capacitor C44 is connected between its gate and source electrodes. The source electrodes of transistors T42 and T46 are connected to the negative supply rail 44. The drain electrode of transistor T44 is connected via a switch S45 to the junction of the drain electrode of transistor T45 and a current source 45 whose other end is connected to the negative supply rail 44. The drain electrode of transistor T47 is connected to an output terminal 47 and via a current source 46 to the negative supply rail 44. The source electrodes of transistors T44, T45, and T47 are connected to the positive supply rail 43.

Transistors T41 and T42 are arranged to have the same gate width/length ratios so that a 1:1 current ratio exists between them. Similarly transistors T43 and T44 are arranged to have the same gate width/length ratio. However, the gate width/length ratio of transistor T45 is arranged to be (1-B) times that of transistor T43 while that of transistor T47 is arranged to be A times that of transistor T43. The current source 42 is arranged to produce a current j , while current source 45 produces a current $(1-B)j$ and current source 46 produces a current Aj . Switches S41 and S42 are closed during portion $\bar{\phi}$ of each sampling period while switches S43, S44, and S45 are closed during portion ϕ of each sampling period.

The principle of operation is similar to that of the ideal integrator described with reference to Figure 3 except that during the ϕ portion of each sampling period an additional current (1-B) is produced by transistor T45 and is passed by switch S45 to the input of the third current memory cell (transistor T46, switch S44, and capacitor C44). During the $\bar{\phi}$ portion of a sampling period this current is inhibited as switch S45 is open and hence the feedback current becomes $B.i$. To create the current $B.i$, the correct matching between transistors T43 and T45 and the correct removal of the bias current (1-B) j is relied upon. However these errors now effect the factor (1-B) which is normally significantly smaller than the factor B. The major problem with the approach shown in Figure 1 arises when B is close to one.

The current sources 45 and 46 may be replaced by the output branches of a current mirror or current memory circuit whose input branch is formed by transistor T46. The transistors in the output branches would be dimensioned to give current ratios of 1:1-B:A. This has the advantage that mismatch errors between transistors T43, T45 and T47 which are not compensated by the described correction of the feedback signal are reduced as the error current in the transistor T46 is then mirrored through into the output branches.

Figure 5 shows a first embodiment of a generalised lossy integrator according to the invention which is similar in form to that of the ideal integrator shown in Figure 4 and in which the same references have been used for equivalent elements. The embodiment shown in Figure 5 has an additional input 48 which is connected via a first switch S48 to the junction of the current source 42 and the drain electrode of transistor T41 and via a second switch S49 to the junction of the drain electrodes of transistors T42 and T43.

In operation a current i is applied to terminal 41 while a current $-i$ is applied to terminal 48. Switch S41 is operated by a signal FE. $\bar{\phi}$ (FE standing for Forward Euler) while switches S48 and S49 are operated by a signal BE. ϕ (BE standing for Backward Euler). When BE = FE = 1 a bilinear integrator is formed. During the portion $\bar{\phi}$ of sampling period (n-1) the current I_a through transistor T41 is given by

$$\begin{aligned}
 I_a &= j - i(n-1) + i_f \\
 \text{where } i_f &= \frac{i_o(n-1)}{A} - \frac{(1-B) i_o(n-1)}{A} \\
 &= \frac{B i_o(n-1)}{A}
 \end{aligned}$$

$$\text{Therefore } I_a = j - i(n-1) + \frac{B i_o(n-1)}{A}$$

15 During the portion ϕ of sampling period n the current i_f is given by
 $i_f = I_a - j - i(n) = i_o(n)/A$.
 Therefore

$$\begin{aligned}
 \frac{i_o(n)}{A} &= j - i(n-1) + \frac{B i_o(n-1)}{A} - j - i(n) \\
 \frac{i_o(n)}{A} - \frac{B i_o(n-1)}{A} &= -i(n) - i(n-1). \\
 \frac{i_o(z)}{A} - \frac{B i_o(z)z^{-1}}{A} &= -i(z) - i(z)z^{-1} \\
 H(z) = \frac{i_o(z)}{i(z)} &= -A \frac{(1+z^{-1})}{1-Bz^{-1}}
 \end{aligned}$$

which is the expression for lossy bilinear integration.

35 The feedback signal i_f and the output signal i_o assume the correct value during the portion ϕ of each sampling period and remain so for the rest of the sampling period. Thus the output signal is valid for all but the settling time of the integrator circuit.

Figure 6 shows a second embodiment of a generalised lossy integrator according to the invention which is similar in form to that of the ideal integrator shown in Figure 4 and in which the same reference signs have been used for equivalent elements. The embodiment shown in Figure 6 has an additional input 49 which is connected via a switch S47 to the junction of the current source 42 and the drain electrode of transistor T41.

In operation a current i is applied to input 41 and a current i is applied to input 49. The switch S41 is closed by a signal FE. ϕ while the switch S47 is closed by a signal BE. ϕ . When BE = FE = 1 a bilinear integrator is formed. The operation as a bilinear integrator is as follows. During portion ϕ of sampling period (n-1) the output current $i_o(n)$ is given by

$$i_o(n) = A(I_a - j)$$

where I_a is the current through transistor T41.

Also

$$i_f(n-1) = \frac{i_o(n-1)}{A} - i(n-1).$$

55 During portion ϕ of sampling period n the feedback current $i_f(n)$ is given by
 $i_f(n) = i_f(n-1) - \frac{1-B}{A} i_o(n-1)$

$$= \frac{B}{A} i_o(n-1) - i(n-1).$$

and the current $i_a(n)$ through transistor T41 is given by

$$i_a(n) = j - i(n) + i_f(n)$$

$$= j - i(n) + \frac{B}{A} i_o(n-1) - i(n-1).$$

5 During portion ϕ of sampling period n the output current $i_o(n)$ is given by

$$i_o(n) = A (i_a(n) - j)$$

$$= A (-i(n) + \frac{B}{A} i_o(n-1) - i(n-1))$$

$$i_o(n) - B i_o(n-1) = -A (i(n) - i(n-1))$$

Converting to z domain

$$10 \quad i_o(z) (1 - Bz^{-1}) = -A i(z)(1 + z^{-1}).$$

$$H(z) = \frac{i_o(z)}{i(z)} = -A \cdot \frac{1 + z^{-1}}{1 - Bz^{-1}}$$

15

which is the expression for a lossy bilinear integrator.

In this case the output signal i_o is not valid until the ϕ portion of each sampling period but only a single differential input is required.

20 Figure 7 shows a fully balanced lossy bilinear integrator using two interconnected integrators as described with reference to Figure 6. The integrator has a first input 141 which is connected to the junction of a current source 142 whose other end is connected to a positive supply rail 143 and the drain electrode of an n-channel field effect transistor T141 via a switch S141 and to the junction of a current source 242 whose other end is connected to the positive supply rail 143 and the drain electrode of an n-channel field effect transistor T241 via a switch S241. A second input 149 is connected via a switch S149 to the junction of the current source 142 and the drain electrode of transistor T141 and via a switch 249 to the junction of current source 242 and the drain electrode of transistor T241. The drain electrode of transistor T141 is connected via a switch S142 to its gate electrode and to the gate electrode of an n-channel field effect transistor T142. A capacitor C142 is connected between the gate and source electrodes of transistor T142. The drain electrode of transistor T142 is connected to the drain and gate electrodes of a p-channel field effect transistor T143 and to one side of a switch S143 whose other side is connected to the gate electrodes of four further p-channel field effect transistor T144, T145, T147, and T150. A capacitor C143 is connected between the gate and source electrodes of transistor T144. The drain electrode of transistor T144 is connected to the drain electrode of transistor T141, to the drain electrode of an n-channel field effect transistor T146, and to one side of a switch S144 whose other side is connected to the gate electrode of transistor T146. A capacitor C144 is connected between the gate and source electrodes of transistor T146.

The drain electrode of transistor T145 is connected to the drain electrode of an n-channel field effect transistor T152 and via a switch S145 to the drain electrode of transistor T146. The drain electrode of transistor T150 is connected to the drain and gate electrodes of an n-channel field effect transistor T151 while the drain electrode of transistor T147 is connected to an output terminal 147 and to the drain electrode of a n-channel field effect transistor 153. The source electrodes of transistors T141, T142, T146, T152, T151, and T153 are connected to a negative supply rail 144 while the source electrodes of transistors T143, T144, T145, T150, and T147 are connected to the positive supply rail 143.

45 The drain electrode of transistor T241 is connected via a switch S242 to its gate electrode and to the gate electrode of an n-channel field effect transistor T242. A capacitor C242 is connected between the gate and source electrode of transistor T242. The drain electrode of transistor T242 is connected to the drain and gate electrodes of a p-channel field effect transistor T243 and via a switch S243 to the gate electrode of four p-channel field effect transistors T244, T245, T250, and T247. A capacitor C243 is connected between the gate and source electrodes of transistor T244. The drain electrode of transistor T244 is connected to the drain electrode of transistors T246 and T241. A switch S244 is connected between the gate and drain electrodes of transistor T246 while a capacitor C244 is connected between its gate and source electrodes. The drain electrode of transistor T245 is connected to the drain electrode of an n-channel field effect transistor T252 and via a switch S245 to the drain electrode of transistor T246. The drain electrode of transistor T250 is connected to the drain and gate electrodes of an n-channel field effect transistor T251 while the drain electrode of transistor T247 is connected to an output 247 and to the drain electrode of an n-channel field effect transistor T253. The gate electrodes of transistors T151, T252, and T253 are connected together as are the gate electrodes of transistors T152, T153, and T251. The source

electrodes of transistors T243, T244, T245, T250, and T247 are connected to the positive supply rail 143 while the source electrodes of transistors T241, T242, T246, T252, T251, and T253 are connected to the negative supply rail 144.

Transistors T141 and T142, switch S142, and capacitor C142 form a first current memory cell having a current ratio of 1:1; transistors T143, T144, T145, T150, and T147, switch S143 and capacitor C143 form a second current memory cell having current ratios 1:1:(1-B)/2:1:A/2; transistors T241 and T242, switch S242, and capacitor C242 form a fourth current memory cell having a current ratio of 1:1; and transistors T243, T244, T245, T250, and T247, switch S243, and capacitor C243 form a fifth current memory cell having current ratios 1:1:(1-B)/2:1:A/2. Transistor T146, switch S144, and capacitor C144 form a third current memory cell while transistor T246, switch 244, and capacitor C244 form a sixth current memory cell. Transistors T151, T253, and T252 form a first current mirror circuit having current ratios 1:A/2:(1-B)/2 while transistors T251, T153, and T152 form a second current mirror circuit having current ratios 1:A/2:(1-B)/2. As before the current sources 142 and 242 both supply the current j .

It will be readily apparent to the person skilled in the art that the integrator shown in Figure 7 is effectively two of the integrators shown in Figure 6 interconnected to receive and produce differential currents thus minimising common mode distortions. The current sources 45 and 46 of Figure 6 are replaced by appropriate output branches of the first and second current mirror circuits. An analysis of the operation of this circuit can be carried out in a similar manner to that given with reference to Figure 6.

Figure 8 shows an embodiment of an integrator circuit in which signal currents pass only through n-channel field effect transistors. The integrator shown uses a forward Euler transform but backward Euler and bilinear integrators could be constructed by appropriate modification of this circuit as would be apparent to persons skilled in the art. The integrator shown in Figure 8 has an input 80 which is connected via a switch S80 to the junction of a current source 81 whose other end is connected to a positive supply rail 88 and the drain electrode of an n-channel field effect transistor T81. A switch S81 is connected between the drain electrode of transistor T81 and its gate electrode and the gate electrode of a further n-channel field effect transistor T82. A capacitor C81 is connected between the gate and source electrodes of transistor T82. The drain electrode of transistor T82 is connected to the positive supply rail 88 via a current source 82 and to the drain and gate electrodes of an n-channel field effect transistor T83. The gate electrode of transistor T83 is connected to the gate electrode of an n-channel field effect transistor T84 via a switch S83. A capacitor C83 is connected between the gate and source electrodes of transistor T84. The drain electrode of transistor T84 is connected to the drain electrode of transistor T81, to the positive supply rail via a current source 83, and to the drain electrode of an n-channel field effect transistor T85. A switch S85 is connected between the drain and gate electrodes of transistor T85 while a capacitor C85 is connected between its gate and source electrodes. The gate electrode of transistor T84 is connected to the gate electrodes of two further n-channel field effect transistors T86 and T87 whose drain electrodes are connected to the positive supply rail 88 via current sources 86 and 87, respectively. The drain electrode of transistor T86 is connected to an output terminal 85 while the drain electrode of transistor T87 is connected via a switch S87 to the drain electrode of transistor T84. The source electrodes of transistor T81 to T87 are connected to a negative supply rail 89.

The current sources 81 and 83 provide a current j , the current source 82 provides a current $2j$, the current source 86 provides a current $A.j$ and the current source 87 provides a current $(1-B)j$. The switches S80 and S81 are closed during the portion $\bar{\phi}$ of each sampling period while the switches S83, S85, and S87 are closed during the portion ϕ of each sampling period. The first current memory cell comprising transistors T81 and T82, switch S81, and capacitor C81 has a 1:1 current ratio. The current ratios of the second current memory cell which comprises transistors T83, T84, T86, and T87, switch S83, and capacitor C83 are 1:1:A:(1-B). The third current memory cell comprises transistor T85, switch S85 and capacitor C85.

The operation of the circuit will first be explained on the assumption that it operates as an ideal integrator i.e. that switch S87, current source 87, and transistor T87 are omitted.

During portion $\bar{\phi}$ of sampling period (n-1) the current I_1 through transistor T81 is given by

$$I_1 = i(n-1) - i_t + j$$
 where $i(n-1)$ is the input current in sampling period (n-1)
 and $i_t = i_o(n-1)/A$

During portion ϕ sampling period n the current I_2 through transistor T83 is given by

$$I_2 = 2j - I_1 = I_3 = \frac{i_o(n) + Aj}{A}$$

where i_3 is the current through transistor T84

$$i_o(n)/A + j = 2j - [i(n-1) - i_o(n-1)/A + j].$$

$$i_o(n) = -A i(n-1) + i_o(n-1)$$

Converting to the z domain

$$5 \quad i_o(z) - i_o(z)z^{-1} = -A i(z)z^{-1}$$

$$10 \quad H(z) = \frac{i(z)}{i_o(z)} = -A \frac{z^{-1}}{1-z^{-1}}$$

This is the expression for a forward Euler integrator.

15 If we now consider the effect of the third current memory cell it can be seen that during the portion ϕ of each sampling period transistor T81 is a current source producing the current $i(n-1) + i_f + j$. Any mismatches between devices which would cause the current i_f to be in error will be compensated for by the third current memory cell as the error current will flow into transistor T85 and when switch S85 opens at the end of portion ϕ the error current will be subtracted from the feedback current.

20 Clearly backward Euler and bilinear integrators could be constructed using this technique and a lossy integrator is formed by subtracting $(1-B)(i_3 - j)$ so that $B(i_3 - j)$ is fed back. This is achieved by means of the switch S87, transistor T87, and current source 87 which causes the current $(1-B)(i_3 - j)$ to be subtracted from that stored in the third current memory cell during the ϕ portion of the sampling period and consequently during the $\bar{\phi}$ portion the current $B(i_3 - j)$ is fed back. Also a fully differential form of all these integrators can be constructed in a manner which will be readily apparent to persons skilled in the art. For

25 an example of a fully differential bilinear integrator reference should be made to our co-pending application no. 8828667.9 (PHB33514) the contents of which are hereby incorporated by reference. Clearly an all p-channel rather than all n-channel embodiment could be constructed which would be of substantially the same form with the polarities reversed.

30 It should be noted that the current memory cells and current mirror circuits shown have been disclosed in their simplest basic form. If an improved performance is required a number of enhancements can be employed. This includes using cascoded current mirrors or current memories, using source degeneration resistors, using dynamic element matching, and using current conveyors or current conveyor type current memory cells particularly where current summing occurs at an input. These techniques are disclosed in one or more of our co-pending applications nos. 8721758 (PHB33385), 8721759 (PHB33386), 8729987 (PHB33426), 8815668.2 (PHB33477), 8828666.1 (PHB33512), 8828668.7 (PHB33513), 8828667.9 (PHB33514), 8903705.5 (PHB33532), and 8903704.8 (PHB33533), the contents of which are hereby

35 incorporated by reference.

From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the design and use of electrical or electronic circuits and component parts thereof and which may be used instead of or in addition to

40 features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the novel feature or any novel combination of features disclosed herein explicitly or implicitly or any generalisation of one or more of those features which would be obvious to persons skilled in the art, whether or not it relates to the same invention

45 as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as does the present invention. The applicants hereby give notice that new claims may be formulated to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

50 Claims

1. An integrator circuit for integrating an input signal in the form of a sampled analogue current, the integrator comprising input means for receiving the input signal, output means for producing as an output

55 signal the integrated input signal, a current memory cell for producing at its output during a first portion of each sampling period a current related to that applied to its input during a second portion of that or a preceding sampling period, means for coupling the output of the current memory cell to the integrator output means, and feedback means for applying a feedback signal to the input of the current memory cell

during the second portion of each sampling period characterised in that the feedback means comprises determining means for determining during the first portion of each sampling period the signal current applied to the current memory cell and means for applying a feedback current dependent on the determined current to the input of the current memory cell during the second portion of each sampling period.

5 2. An integrator circuit as claimed in Claim 1 in which the determining means comprises means for producing a current at the input of the current memory cell during the first portion of each sampling period which is equal to the current applied to the input of the current memory cell during the second portion of that or a preceding sampling period.

10 3. An integrator circuit as claimed in Claim 2 in which the current memory cell comprises a field effect transistor having a switch connected between its drain and gate electrodes, the switch being closed only during the second portion of each sampling period.

4. An integrator as claimed in Claim 3 in which an additional capacitor is connected between gate and source electrodes of the transistor.

15 5. An integrator circuit as claimed in any preceding claim in which the means for coupling the output of the current memory cell to the output means of the integrator circuit comprises a further current memory cell.

20 6. An integrator circuit as claimed in Claim 5 in which the means for applying the feedback current comprises means for coupling an output of the second current memory cell to the input of the first current memory cell during the second portion of each sampling period.

25 7. An integrator circuit as claimed in Claim 6 in which the input of a third current memory cell is coupled to the input of the first current memory cell, the third current memory cell receiving during the first portion of each sampling period the difference between the current produced at the input of the first current memory cell and that produced at the output of the second current memory cell, and supplying that current to the input of the first current memory cell during the second period of each sampling period.

8. An integrator circuit as claimed in Claim 7 in which the second current memory cell has a further output which supplies a scaled version of the current at the first output during the first portion of each sampling period and applies it to the input of the third current memory cell.

30 9. An integrator as claimed in any preceding claim further comprising means for adding a bias current to the input signal and means for subtracting a suitably scaled bias current from the feedback and output signals so that bi-directional input currents can be integrated and bi-directional output currents produced.

10. An integrator circuit as claimed in any preceding claim in which signal currents are conducted only by field effect transistors of one polarity.

35 11. An integrator circuit as claimed in Claim 10 in which signal currents are conducted only by n-channel field effect transistors.

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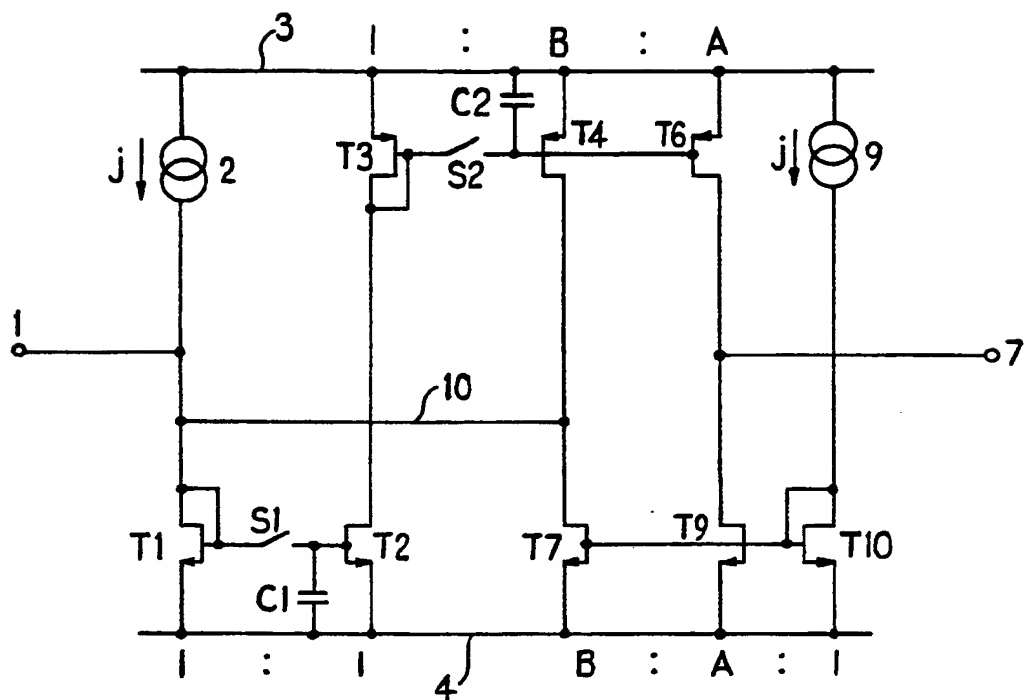


FIG.1

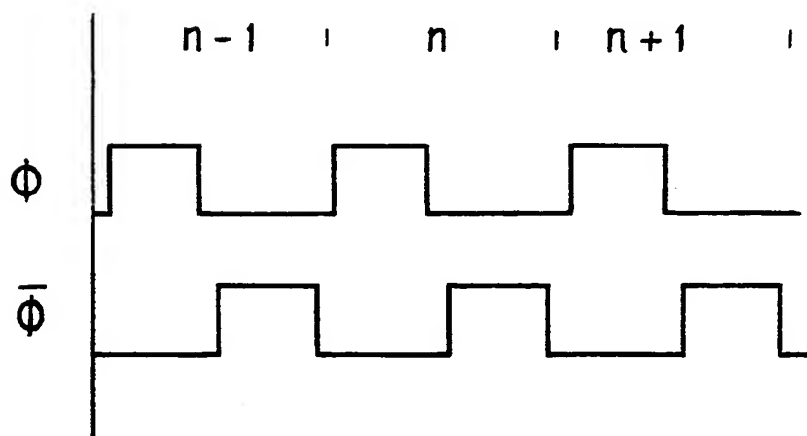


FIG.2

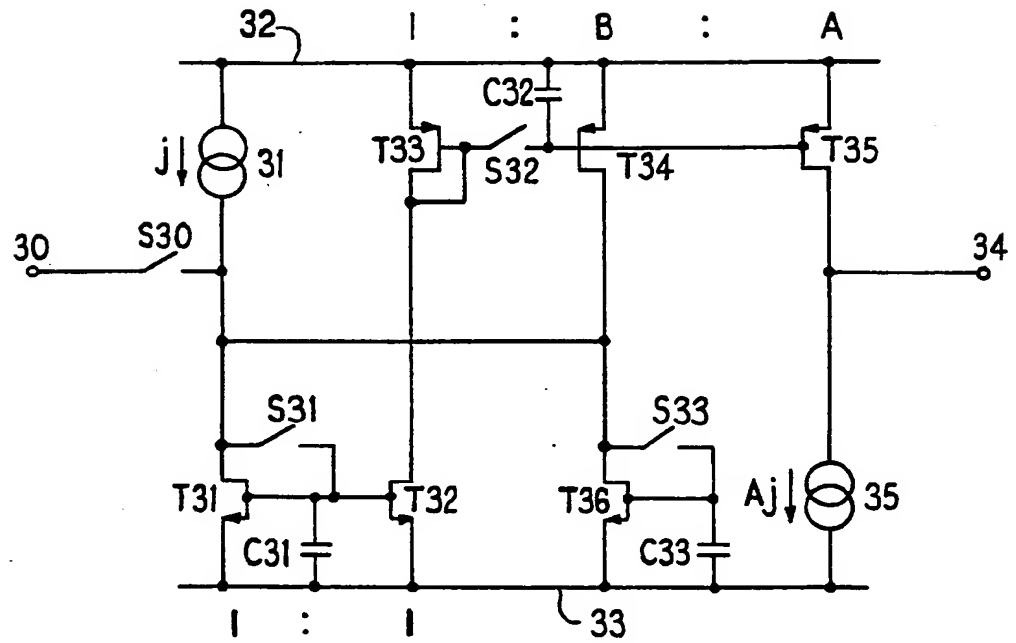


FIG. 3

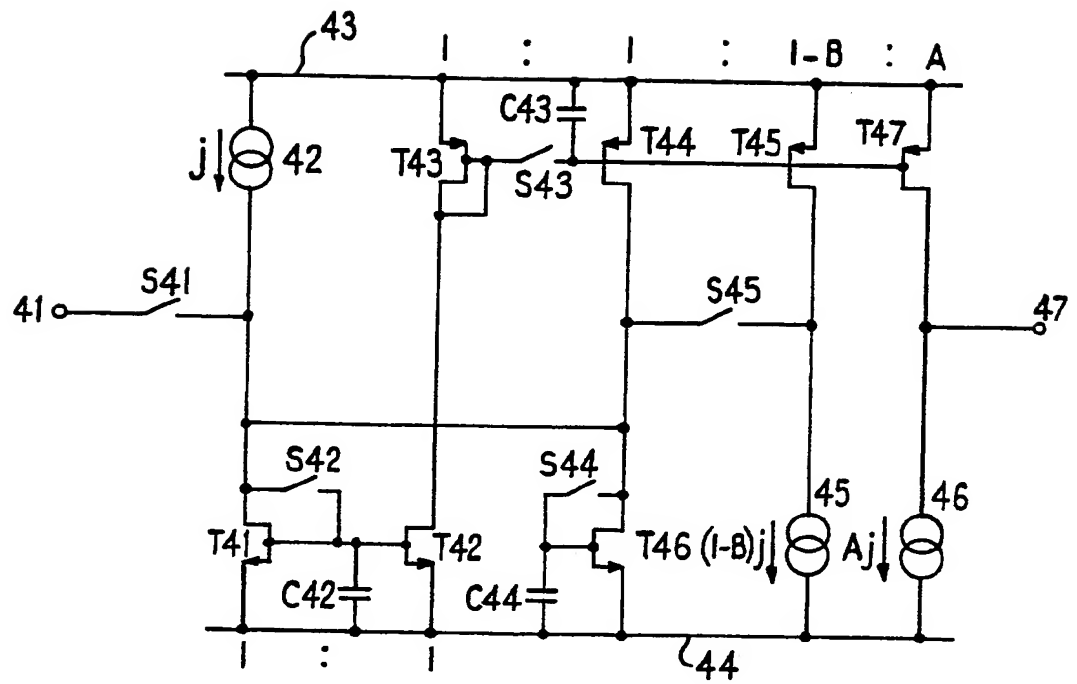


FIG.4

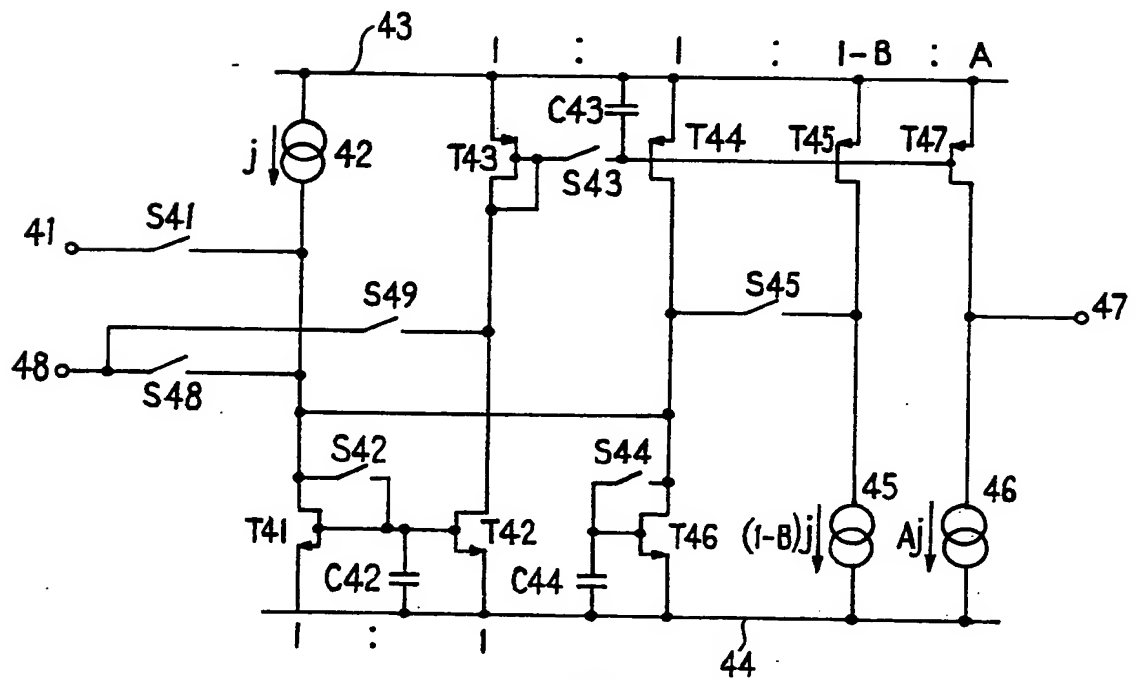


FIG.5

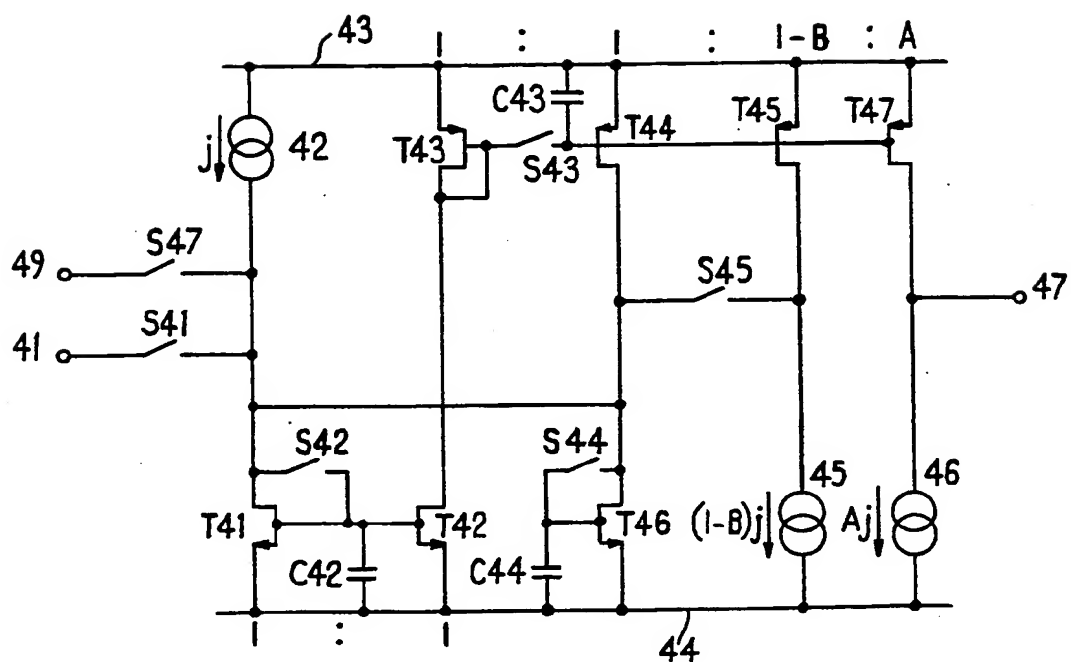


FIG. 6

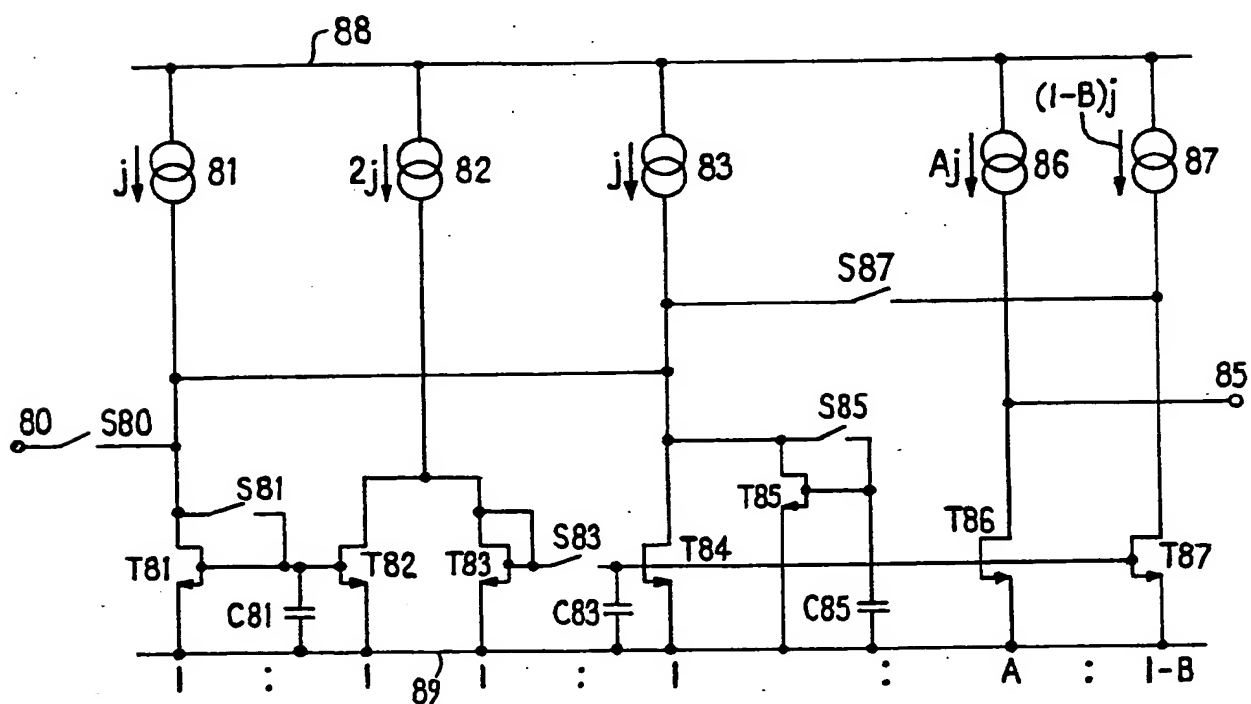


FIG. 8

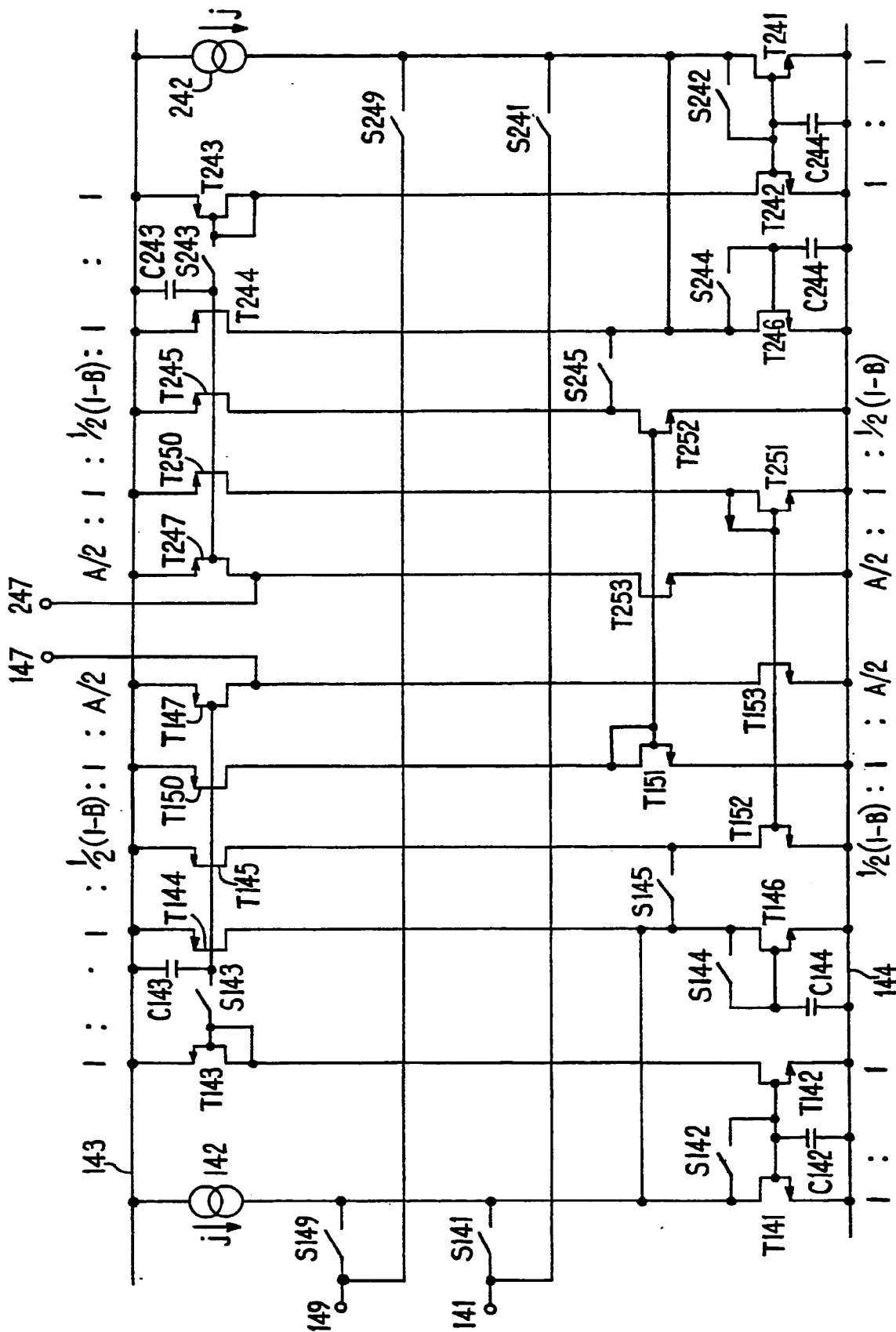


FIG.7



DOCUMENTS CONSIDERED TO BE RELEVANT			EP 90201130.3
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. ⁴)
X	<u>EP - A2 - 0 308 008</u> (PHILIPS) * Abstract; column 17, line 51 - column 8, line 50, fig. 2,3 *	1-11	G 06 G 7/18
X	<u>EP - A2 - 0 308 007</u> (PHILIPS) * Abstract; column 6, line 6 - column 9, line 9; fig. 2-5 *	1-11	
			TECHNICAL FIELDS SEARCHED (Int. Cl. ⁴)
			G 06 G H 03 K
The present search report has been drawn up for all claims			
Place of search VIENNA		Date of completion of the search 31-08-1990	Examiner NEGWER
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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